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SRI VASAVI ENGINEERING COLLEGE

(Sponsored by Sri Vasavi Educational Society)
Approved by AICTE, New Delhi and Permanently Affiliated to JNTUK, Kakinada
Pedatadepalli, **TADEPALLIGUDEM – 534 101,** W.G. Dist, (A.P.)

Department of Electronics and Communication Engineering

STLD QUESTION BANK

UNIT –I

1) Explain the different types of number systems.

2) Convert the following numbers from one radix to another radix

i) $(1001101)_2 = (\ )_8$
ii) $(1001101.11)_2 = (\ )_{10}$
iii) $(1001101)_2 = (\ )_{16}$
iv) $(1110)_2 = (\ )_{grey}$
v) $(7241)_8 = (\ )_{10}$
vi) $(ABC152.12)_{16} = (\ )_{10}$
vii) $(ABC152.12)_{16} = (\ )_2$
viii) $(9762)_{10} = (\ )_2$
ix) $(9762)_{10} = (\ )_8$
x) $(9762)_{10} = (\ )_{16}$

3) a) Perform $(28)_{10} - (15)_{10}$ using 1's complement representation.
b) Perform $(15)_{10} - (28)_{10}$ using 1's complement representation.
c) Perform $(28)_{10} - (15)_{10}$ using 2's complement representation.
d) Perform $(15)_{10} - (28)_{10}$ using 2's complement representation.

UNIT –II

1) Draw and explain concept of k maps up to 6 variables i.e.,(1,2,3,4,5,6 variables) with maps for SOP and POS forms.

2) Reduce the following functions by using k-map method

$$Y=\bar{A}\bar{B}\,C\bar{D} + ABC\bar{D} + A\bar{B}C\bar{D} + A\bar{B}CD + A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}\bar{C}\bar{D}$$

$$f(ABCD) = \sum m(1,3,7,11,15) + \sum d(0,2,4)$$

$$F(A,B,C,D) = \prod M(0,2,6,7,8,12,13) + \prod d(3,5,10,14)$$

3) Simplify the following function using Quine Mecluskey method

$F(A,B,C,D) = \sum m(0,2,3,6,7,8,10,12,13)$
$F(A,B,C,D) = \sum m(0,2,6,7,8,12,13) + \sum d(3,5,10,14)$

4) Design 4 bit binary to BCD converter using K-Map

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UNIT-III

1. Design of half adder, half subtractor by using basic gates and universal gates with necessary expressions.

2. Design full adder& full subtractor by using universal gates and using two half sub tractors basic half adders with necessary Boolean functions.

3. Design and 2-bit and 4-bit digital comparator.

4. a) Implement 4:16 decoder using two 3:8 decoders.
   b) Explain the operation of decoder implement 5:32 decoder using IC 74138 and 74139

5. a) Explain operation of multiplexer and DEMUX with truth table with example.
   b) Design 1:16 MUX by using 1:4 MUX and design 16:1 DEMUX by using 4:1 DEMUX with OR gate.

6. a)Design Ex-3 and BCD adders with example
   b) Draw and explain look-ahead adder and priority encoder.

UNIT-IV

1. a)Difference between PROM, PLA & PAL
   b)Explain architecture of PROM, PLA, PAL

2. BCD to Ex-3 code converter using PROM,PLA,PAL using programming tables.

3. Implement the following function using PLA, PAL using programming tables.
   $F1=\sum m(0,2,4,6,8,9,15)$
   $F2=\sum m(1,5,7,3,6,9,14,15)$

4. Design 64:4 PROM and design the PLA programming table for a combinational circuit that squares a 3-bit number.

5. Implement the following Boolean function using PROM
   $F1(A1,A0)=\sum m(1,2)$ $F2=(A1,A0)=\sum m(0,1,3)$

6. Illustrate how a PLA can be used for combinational logic design with reference to functions.
   $F1(a, b, c)=\sum m(0,1,3,4)$
   $F2(a,b,c)=\sum m(1,2,3,4,5)$

UNIT-V

1. a) Comparison between sequential circuit and combinational logic circuits.
   b) Difference between synchronous and asynchronous circuits

2. a) Design SR-latch, T-latch , D-latch with truth tables and logic diagrams
   b) Draw and explain the operation of Master Slave JK flip-flop and JK flip-flop with truth tables.

3. Convert the following flip-flops with excitation tables
   a) SR to D-flip-flop
   b) D to SR-flip-flop
   c) JK to D-flip-flop
   d) JK to SR-flip-flop
   e) D to T-flip-flops

4. a) Design the 3-bit asynchronous counter with wave forms
   b) Design the 2-bit synchronous counter with wave forms

5. Design and explain the operations of following counters
   a) Ring counter
   b) Johnson counters

6. a)Design of registers and draw and explain the various types of shift registers(SISO,SIPO,PIPO,PISO)

7. Draw and explain operation of following registers
   a) Bi-directions shift registers
   b) Universal shift registers

UNIT-VI

1. Explain the following related to sequential circuits with suitable examples.
   a)State diagram
   b)State table
   c) state assignment
   d)Distinguish between Melay & Moore machines

2. a)Draw the Diagram of melay-type FSM for serial adder
   b)Draw the logic diagram of Melay & Moore model & explore its operation with examples

3. a) Convert the following melay machine into a corresponding moore machine.

P.S	NS,X=0	Z, X=1
A	B,0	E,0
B	E,0	D,0

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C	D,1	A,0
D	C,1	E,0
	B,0	D,0

b)A sequential circuit has one i/p & one o/p .the state diagram is shown below. Design sequential circuit with
(a) D flip flop (c) RS flip flop

4. a) Explain about lockout condition in counter
b) Design a synchronous counter for 4 ---> 6---> 7----->3---->1 ---> 4 .Avoid lock out condition, use JK type design.

5. A locked sequential circuit is provided with a single input X and single out put Z. whenever the input produce a string of pulses 111 & 000 ∑ at end of sequence it produces an o/p z=1 & overlapping is also required.
a) Obtain state diagram
b) Obtain state tables

6. a)Design a melay type sequence detector to detect a serial input sequence of 101
b) Design a moore type sequence detector to detect a serial input sequence of 111