ACADEMIC REGULATIONS
COURSE STRUCTURE
AND
DETAILED SYLLABUS

ELECTRONICS & COMMUNICATION ENGINEERING

BRANCH

For

M.Tech

(VLSI & Embedded Systems)

Academic Year 2018-19

SRI VASAVI ENGINEERING COLLEGE (AUTONOMOUS)

(Sponsored by Sri Vasavi Educational Society)
Approved by AICTE, New Delhi and Permanently Affiliated to JNTUK, Kakinada
Pedatadepalli, **TADEPALLIGUDEM – 534 101,** W.G. Dist, (A.P.)

ACADEMIC REGULATIONS

Rules & Regulations for Award of M.Tech:

The M.Tech Degree of Sri Vasavi Engineering College (Autonomous), Pedatadepalli, Tadepalligudem, under Jawaharlal Nehru Technological University Kakinada shall be conferred on candidates who are admitted to the program and fulfill all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS:

Admission to the above program shall be made subject to eligibility criteria, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates at the Qualifying Examination/Entrance Test conducted by the University / Government or on the basis of any other order of merit as approved by the University/ Government subject to reservations as laid down by the Govt. from time to time.

1.1 ADMISSIONS UNDER SPECIAL CASES:

These may arise in the following situations.

1. When a student gets detained due to academic regulations and re-joins the college to complete the programme in a new regulation.
2. When a student discontinues for some time and re-joins the college to complete the programme in a new regulation.
3. When a student seeks transfer from other colleges to SVEC and intends to pursue M.Techprogramme in the eligible branch of study.

These admissions may be permitted by the College Academic Council as per the norms stipulated by the statutory bodies and the Government of Andhra Pradesh from time-to-time.

In all such cases for admission if necessary permissions from the statutory bodies are to be obtained and the programme of study at the college will be governed by the transitory regulations stipulated in **12.0.**

An under taking from the students is to be taken at the time of admission stating that they would abide by the transitory regulations specified by the authorities if there is any change in the regulations.

2.0 AWARD OF M.TECH DEGREE:

i. A student shall be declared eligible for the award of the M. Tech Degree, if he pursues

program of study in not less than two and not more than four academic years.

ii. The student shall register for all 70 credits and secure all the 70 credits.

iii. The minimum instruction days in each semester are 90.

3.0 Specialization:

The following specializations are offered at present for the M. Tech program

a) M.Tech- Structural Engineering
b) M.Tech- Power System Control & Automation
c) M.Tech- Machine Design
d) M.Tech- VLSI & Embedded Systems
e) M.Tech- Computer Science & Engineering

4.0 ATTENDANCE:

A student is eligible to write the semester end examinations (SEE) if he/she acquires a minimum of 75% of attendance in aggregate of all the courses of that semester put together.

4.1 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in a given semester may be granted by the College Academic Committee on medical grounds provided the student has submitted the application for medical leave along with medical certificate from a medical practitioner within three days form reporting to the class work after the expiry of the medical leave. However, a student can avail this concession on medical grounds for not more than once during entire duration of the program.

4.2 Condonation of shortage of attendance below 75% and above 65% may also be considered by the college academic committee in case of students who represent the college in approved extracurricular activities such as sports, games, cultural meets, seminars, workshops, conferences outside the college provided they have obtained prior written permission from Head of the Department concerned and also submitted the certificate of participation from the organizer of the event within three days after the completion of the event.

4.3 A stipulated fee shall be payable towards condonation of shortage of attendance.

4.4 Attendance below 65% in aggregate shall not be condoned under any circumstances.

4.5 Students whose shortage of attendance is not condoned in any semester are not eligible to write their semester end examinations.

4.6 A student who is in short of attendance in a semester may seek re-admission into that semester when offered again, within 1 week from the date of the commencement of class work.

4.7 A student will be promoted to the next semester if he satisfies the attendance requirement of the present semester.

4.8 If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

5.0 EVALUATION:

The performance of the candidate in each semester shall be evaluated course-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation (IE) and End Semester Examination.

Theory Courses:

i. For the theory courses 60 marks shall be awarded based on the performance in the End Semester Examination and 40 marks shall be awarded based on the Internal Evaluation. The internal evaluation shall be made based on the weighted average of the marks secured in the two Mid Term-Examinations conducted-one in the middle of the Semester and the other immediately after the completion of instruction.

ii. Each Mid-term examination shall be conducted for 40 marks and duration of 120 minutes with 4 questions (without choice), each question for 10 marks.

The weighted average is computed is as follows:

Internal Evaluation= Best performance x 0.7 + Performance in the other examination x 0.3

End Semester Examination shall be conducted for 60 marks.

There will be 5 questions with internal choice covering the entire syllabus. The student has to answer all the questions.

Practical Courses:

iii. For practical course, 60 marks shall be awarded based on the performance in the End Semester Examination (Conducted by External Examiner and Internal Examiner) and

40 marks shall be awarded based on the day-to-day performance and an Internal Test as Internal Evaluation.

Seminar:

iv. There shall be two seminar presentations one in I semester and another in II semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before a Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation for 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

MOOCS Courses:

v. Every student has to register for a MOOCs course in 1st semester itself as approved by the Departmental Committee and complete it on self study basis and submit the certificate of successful completion before the end of 3rd semester.

Comprehensive Viva:

vi. Every Student has to appear for a comprehensive Viva-Voce at the end of III Semester. The performance will be assessed by a committee for 50 marks.

vii. A candidate shall be deemed to have secured the minimum academic requirement in a

courseif he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

viii. **In case the candidate does not secure the minimum academic requirement in any course (as specified in 5 (vii)) he has to reappear for the End Semester Examination in that course.**

ix. **A candidate shall be given one chance to re-register for each course provided the internal marks secured by a candidate are less than 50% and has failed in the end examination. In such a case, the candidate must re-register for the course(s) and secure the required minimum attendance. The candidate's attendance in the re-registered course(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those course(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stands cancelled.**

x. **For re-registration the candidates have to apply to the Dean Academics by paying the requisite fees and get approval from the College before the start of the Semester in which re-registration is required.**

In case the candidate secures less than the required attendance in any re-registered course(s), he shall not be permitted to write the End Examination in that course. He shall again re-register the course when next offered.

6.0 EVALUATION OF PROJECT/DISSERTATION WORK:

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

i. A Project Review Committee (PRC) shall be constituted with Head of the Department and two other senior faculty members.

ii. **The project work is carried out in two parts. i) Part-A & ii) Part-B**

Part-A is evaluated internally at the end of 3rd semester for 50 marks out of which 25 marks are awarded by the supervisor and 25 marks are awarded by the committee.

The total project work is evaluated at the end of 4th semester for a total of 100 marks out of which 50 marks are awarded by an internal committee and 50 marks are awarded by an external examiner.

iii. **Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses, both theory and practical.**

iv. **After satisfying 6 (ii), a candidate has to submit, in consultation with his project supervisor, the title, expected outcomes and plan of action of his project work for approval. The student can initiate the Project work, only after obtaining the approval from the Project Review Committee (PRC).**

If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the Project Review Committee (PRC). However, the Project Review Committee (PRC) shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

v. The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. The candidate has to pass all the theory and practical courses before submission of the Thesis.

vi. Three copies of the Project Thesis certified by the supervisor shall be submitted to the department.

vii. The thesis shall be adjudicated by an External Examiner approved by the Principal from a panel of 4 Examiners, eminent in the field, submitted by the Department.

viii. If the report of the examiner is not favorable, the candidate shall revise and re-submit the Thesis in the time frame as decided by the PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected. The candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the competent authority.

ix. If the report of the examiner is favorable, Viva-Voce examination shall be conducted by the external examiner who adjudicated the thesis and the performance will be graded as follows.

		G.P.
S	Excellent	10
A.	Good	08
B.	Satisfactory	06
	Unsatisfactory	to reappear for the exam

The Head of the Department shall coordinate and make arrangements for the conduct of Viva-Voce examination.

If the report of the Viva-Voce is unsatisfactory, the candidate shall retake the Viva-Voce examination only after three months. If he fails to get a satisfactory report at the second Viva-Voce examination, the candidate has to re-register for the project andcompletethe project within the stipulated time after taking the approval from the College.

7.0 Grading System:

7.1 Based on the students performance in the given semester letter grades will be awarded at the end of the semester for each course. The letter grades and the corresponding grade points are as given in the following table.

Grade	Grade Points	% of marks
S	10	≥ 90
A	9	$\geq 80 - < 90$
B	8	$\geq 70 - < 80$
C	7	$\geq 60 - < 70$
D	6	$\geq 50 - < 60$
F	0 (Failed)	< 50

8.0 GRADE POINT AVERAGE:

Computation of SGPA and CGPA:

The following is the procedure to compute the Semester Grade Point Average (SGPA) for each semester and Cumulative Grade Point Average (CGPA) for all four semesters of the program:

i. The SGPA is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student,i.e

$$\textbf{SGPA}\ (Si) = \sum(Ci \times Gi) / \sum Ci$$

whereCi is the number of credits of the i^{th}course and Gi is the grade point scored by the student in the i^{th}course.

ii. The CGPA is also calculated in the same manner taking into account all the courses undergone by a student over all the semesters of a programme, i.e.

$$\textbf{CGPA} = \sum(Ci \times Si) / \sum Ci$$

Where Si is the SGPA of the ith semester and Ci is the total number of credits in that semester.

The SGPA and CGPA shall be rounded off to 2 decimal places and reported in the transcripts.

Illustration for Computation of SGPA and CGPA:

Computation of SGPA Illustration No.1:

Course	Credit	Grade letter	Grade point	Credit Point (Credit x Grade)
Course 1	3	A	9	3 x 9 = 27
Course 2	3	C	7	3 x 7 = 21
Course 3	3	B	8	3 x 8 = 24
Course 4	3	S	10	3 x 10 = 30
Course 5	3	D	6	3 x 6 = 18
Course 6	3	C	7	3 x 7 = 21
Course 7	2	A	9	2 x 9 = 18
Total	**20**			**159**

Thus, **SGPA at the end of 1st Semester= 159/20=7.95**

Illustration No.2 (with one failure)

Course	Credit	Grade letter	Grade point	Credit Point (Credit x Grade)
Course 1	3	A	9	3 x 9 = 27

Course 2	3	C	7	3 x 7 = 21
Course 3	3	B	8	3 x 8 = 24
Course 4	3	S	10	3 x 10 = 30
Course 5	3	F	0	3 x 0 = 00
Course 6	3	C	7	3 x 7 = 21
Course 7	2	A	9	2 x 9 = 18
Total				**141**

Thus, **SGPA at the end of 1st Semester= 141/20=7.05**

Illustration No.2(a)

Course	**Credit**	**Grade letter**	**Grade point**	**Credit Point (CreditxGrade)**
Course 5	3	D	6	3 x 6=18
Total Credits of the Semester	**20**			Ci(First Attempt)141 +Ci (subsequent attempt) 18= **159**

Thus, **SGPA=159/20=7.95**

Illustration No.3

Second Semester performance:

Course	**Credit**	**Grade letter**	**Grade point**	**Credit Point (Credit x Grade)**
Course 1	3	A	9	3 x 9= 27
Course 2	3	C	7	3 x 7= 21
Course 3	3	B	8	3 x 8 = 24
Course 4	3	Ex	10	3 x 10 =30
Course 5	3	A	9	3 x 9 = 27
Course 6	3	C	7	3 x 7 =21
Course 7	2	A	9	2 x 9 =18
Total	**2**			**168**

Thus, SGPA of 2nd Semester = 168/20=8.4

CGPA at the end 2nd Semester:

$$\text{CGPA}=\frac{20*7.95+20*8.4}{40}=8.175$$

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Sem-1	*Sem-2*	*Sem-3*	*Sem-4*
Credit : 20 SGPA: 7	Credit: 20 SGPA: 8.5	Credit : 10 SGPA: 9.2	Credit : 20 SGPA: 6.86

CGPA after Final Semester:

Thus, CGPA $= \frac{20*7+20*8.5+10*9.2+20*6.86}{70} = 7.70$

AWARD OF CLASS:

A candidate who becomes eligible for the award of M.Tech degree shall be placed in one of the following classes based on CGPA.

TABLE: CGPA REQUIRED FOR AWARD OF DEGREE

Distinction	**≥ 7.75***
First Class	**≥ 6.75**
Second Class	**≥ 6.0**

*In addition to the required CGPA of 7.75, the student must have necessarily passed all thecourses of each semester in the first attempt.

9.0 MALPRACTICES:

The Principal shall refer the cases of malpractices in Continuous Internal Evaluation (CIE) and Semester End Examination (SEE) to an Enquiry Committee constituted by him. The committee will submit a report on the malpractice allegedly committed by the student to the Principal.

Rules pertaining to the punishments in the case of Malpractice are given in Annexure-1

10.0 ADDITIONAL ACADEMIC REGULATIONS:

Grade Sheet: A grade sheet (memorandum) will be issued to each student indicating his performance in all courses taken in that semester and also indicating the grades and SGPA.

Transcripts: After successful completion of the total program of study, a Transcript containingperformance of all academic years will be issued as a final record. Duplicate transcriptswillalso be issued up to any point of study to any student on request and by paying the stipulatedfee in force. Candidates shall be permitted to apply for recounting/revaluation within thestipulated period with payment of prescribed fee. The Academic Council has to approve andrecommend to the JNTUK, Kakinada for the award ofa degree to any student

11.0 Withholding of Results

If the student has not paid the dues, if any, to the university or if any case of indiscipline is pending against him, the result of the student will be withheld. His degree will be withheld in such cases.

12.0 Transitory Regulations:

For students admitted under special cases (mentioned in 1.1) these transitory regulations will provide the modus operandi.

At the time of such admission, based on the Programme pursued (case by case):

1. Equivalent courses completed by the student are established by the BOS concerned.
2. Marks/Credits are transferred for all such equivalent courses and treated as successfully cleared in the Programme of study prescribed by SVEC.
3. A Programme chart of residual courses not cleared will be derived and a Programmeof study with duration specified will be prescribed for pursuit at SVEC.
4. Marks obtained in the previous system if the case be, are converted to grades and CGPA is calculated accordingly.

All other modalities and regulations governing shall be the same as those applicable to the stream of students with whom such a candidate is included into.

Regarding the students who were admitted under JNTU, Kakinada regulations for affiliated colleges:

If they happen to join and study along with their juniors at SVEC, the transitory regulations to be specified by JNTU, Kakinada for such students have to be followed.

13.0 General:

i. Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”,“her”, “hers”.

ii. The academic regulation should be read as a whole for the purpose of any interpretation.

iii. In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.

iv. The University may change or amend theacademic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the University.

COURSE STRUCTURE

Course Structure for

M. Tech (VLSI&ES) w.e.f A.Y 2018-19

I Semester

S. No.	Course Code	Coarse Name	L	T	P	C
1.	V18VLT01	Digital System Design	3	-	-	3
2.	V18VLT02	VLSI Technology And Design	3	-	-	3
3.	V18VLT03	CMOS Analog IC Design	3	-	-	3
4.	V18VLT04	Embedded Systems Design-I	3	-	-	3
5.	V18VLT05 V18VLT06 V18VLT07 V18VLT08	**ELECTIVE-1** Embedded C Digital Signal Processors &Architectures System On Chip Soft Computing Techniques	3	-	-	3
6.	V18VLT09 V18VLT10 V18VLT11 V18VLT12	**ELECTIVE -2** Digital Design Through HDL CPLD & FPGA Architecures And Applications Algorithms For VLSI Design –Automation VLSI Signal Processing	3	-	-	3
7.	V18VLL01	VLSI LAB	-	-	4	2
8.	V18VLL02	SEMINAR-I		-	2	2
			18	-	06	**22**

Total Contact Hours : 24
Total Credits: 22

II Semester

S. No.	Course Code	Coarse Name	L	T	P	C
1.	V18VLT13	Design For Testability	3	-	-	3
2.	V18VLT14	CMOS Digital IC Design	3	-	-	3
3.	V18VLT15	Embedded System Design - II	3	-	-	3
4.	V18VLT16	Embedded Real Time Systems	3	-	-	3
5.	V18VLT17 V18VLT18 V18VLT19 V18VLT20	**ELECTIVE-III** Low Power VLSI CMOS Mixed Signal Circuit Design System Verilog Semiconductor Memory Design And Testing	3	-	-	3
6.	V18VLT21 V18VLT22 V18VLT23 V18VLT24	**ELECTIVE-IV** Hardware Software Co-Design Embedded Computing Design For Internet Of Things Software for Embedded Systems.	3	-	-	3
7.	V18VLL03	Embedded System Design Lab	-	-	4	2

8.	V18VLL04	SEMINAR-II		-	2	2
			18	-	06	**22**

Total Contact Hours : 24
Total Credits: 22

III Semester

S.No	Course Code	Name of the Course	L	P	C
1	V18VLL05	Comprehensive VIVA			2
2	V18VLL06	MOOCs			MNC
3	V18VLL07	Project work	-	-	-
Total Credits					**2**

IV Semester

S.No	**Course Code**	**Name of the Subject**	**L**	**P**	**C**
1	V18VLL07	Project work (Continued)	-	-	24
Total Credits					**24**

Total Credits for PG Programme = 70

SYLLABUS

DIGITAL SYSTEM DESIGN

Course Outcome:

The student will be able to

- Describe the algorithms for minimization of functions
- Describe the algorithms for minimization of PLDs.
- Design large scale digital systems.
- Discuss the fault model and diagnosis in combinational and sequential circuits.

UNIT-I: Minimization Procedures and CAMP Algorithm

Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs, CAMPI algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-II: PLA Design, PLA Minimization and Folding Algorithms

Introduction to PLDs, basic configurations and advantages of PLDs, PLA-Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm (IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT -III: Design of Large Scale Digital Systems

Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT-IV: Fault Diagnosis in Combinational Circuits

Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

UNIT-V: Fault Diagnosis in Sequential Circuits

Fault detection and location in sequential circuits, circuit test approach, initial state identification, Haming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

TEXT BOOKS:

1. Logic Design Theory-N. N. Biswas, PHI
2. Switching and Finite Automata Theory-Z. Kohavi , 2nd Edition, 2001, TMH
3. Digital system Design using PLDd-Lala

REFERENCE BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – MironAbramovici, Melvin A.
Breuer and Arthur D. Friedman- John Wiley & Sons Inc.

VLSI TECHNOLOGY AND DESIGN

Course Outcome:

The student will be able to

- Describe the Microelectronics and MOS Technologies
- Describe various processes in IC Production.
- Sketch the Layout Design.
- Discuss the Floor Planning, Architecture Design.

UNIT-I: Review of Microelectronics and Introduction to MOS Technologies:

MOS, CMOS, Bi-CMOS Technology Trends and Projections Electronic design automation concept, ASIC and FPGA design flows, SOC designs, IC fabrication process.

UNIT-II: IC Production Process - I

Crystal Growth and Wafer Preparation: Introduction, Electronic-Grade Silicon, Czochralski Crystal Growing, Silicon Shaping, Process Considerations, Epitaxy: Introduction, Vapour-Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation.

UNIT-III: IC Production Process – II

Lithography: Introduction, Various Lithography techniques: Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography. Etching Techniques, Deposition Processes, Ion Implantation, Metallization.

UNIT-IV: Layout Design and Tools:

Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

Subsystem Design and Layout: Some architectural issues, switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations.

UNIT-V:

Floor Planning: Introduction**,** Floor planning methods, off-chip connections.

Architecture Design: Introduction, Register-Transfer design, high-level synthesis, architectures for low power, architecture testing.

Chip Design: Introduction and design methodologies.

TEXT BOOKS:

1. S. M. Sze, “VLSI Technology”, McGraw-Hill, Second Edition.

2. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A. Pucknell,SholehEshraghian, 2005, PHI Publications.

3. Modern VLSI Design-Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

1. VLSI Design Technologies for Analog and Digital Circuits, Randall L.Geiger, PhillipE.Allen, Noel R.Strader, TMH Publications, 2010.

2. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming-BO Lin,CRC Press, 2011.

3. Principals of CMOS VLSI Design-N.H.E Weste, K. Eshraghian, 2nd Edition, AddisonWesley.

CMOS ANALOG IC DESIGN

Course Outcome:

The student will be able to

- Describe the concept of MOS device and modeling of MOS drain current for large and small signal anaysis
- Design and analyze Analog CMOS Sub-Circuits.
- Distinguish Large signal and small signal analysis of CMOS Amplifiers
- Describe the CMOS Op-Amps & Applications.

UNIT -I: MOS Devices and Modeling

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II: Analog CMOS Sub-Circuits

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III: CMOS Amplifiers-I

Inverters- Active load inverter, current source inverter, push-pull inverter, Differential Amplifiers- large signal analysis, small signal analysis, design of differential amplifier,

UNIT -IV: CMOS Amplifiers-II

Cascode Amplifiers- Large signal analysis, small signal analysis and frequency response, design of cascade amplifier, Current Amplifiers- single ended input current amplifier, differential input current amplifier, Output Amplifiers- class-a amplifier, source follower, push pull CS amplifier, High Gain Amplifiers Architectures.

UNIT -V: CMOS Op-Amps & Applications

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps,Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp, Characterization of Comparator, Two-Stage comparator design.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, OxfordUniversity Press, International Second Edition/Indian Edition, 2010.

2. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn, 2016.

2.Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewisand R. G. Meyer, Wiley India, Fifth Edition, 2010.

3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

EMBEDDED SYSTEM DESIGN - I

Course Outcome:

The student will be able to

- Describe the basic concepts of an embedded system and its design
- Differentiate the hardware and software components required to develop an embedded system
- Generalize the Embedded System design and development life cycle model and case studies

UNIT-I: Introduction

An Embedded System-Definition, Examples, Current Technologies, Integration in system Design, Embedded system design flow, hardware design concepts, software development, processor in an embedded system and other hardware units, introduction to processor based embedded system design concepts.

UNIT-II: Embedded Hardware

Embedded hardware building blocks, Embedded Processors – ISA architecture models, Internal processor design, processor performance, Board Memory – ROM, RAM, Auxiliary Memory, Memory Management of External Memory, Board Memory and performance. Embedded board Input / output – Serial versus Parallel I/O, interfacing the I/O components, I/O components and performance, Board buses – Bus arbitration and timing, Integrating the Bus with other board components, Bus performance.

UNIT-III: Embedded Software

Device drivers, Device Drivers for interrupt-Handling, Memory device drivers, On-board bus device drivers, Board I/O drivers, Explanation about above drivers with suitable examples, Board support packages, Middleware and Application Software – Middle ware, Middleware examples, Application layer software examples.

UNIT-IV: Embedded System Design, Development, Implementation and Testing

Embedded system design and development lifecycle model, creating an embedded systemarchitecture, introduction to embedded software development process and tools- Host and Targetmachines, linking and locating software, Getting embedded software into the target system,issues in Hardware-Software design and co-design, Implementing the design-The main software utility tool, CAD and the hardware, Translationtools, Debugging tools, testing on host machine, simulators, Laboratory tools, System Boot-Up.

UNIT-V: Embedded System Design-Case Studies

Case studies- Processor design approach of an embedded system, Micro Blaze Processor based Embedded system design on Xilinx platform-NiosII Processor based Embedded system design on Altera platform

TEXT BOOKS:

1. Tammy Noergaard "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier(Singapore) Pvt.Ltd.Publications, 2005.

2. Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & Sons Inc.2002.

REFERENCE BOOKS:

1. Peter Marwedel, "Embedded System Design", Science Publishers, 2007.

2. Arnold S Burger, "Embedded System Design", CMP.

3. Rajkamal, "Embedded Systems: Architecture, Programming and Design", TMH Publications, Second Edition, 2008.

Elective-I EMBEDDED C

Course Outcome:

The student will be able to

- Describe the basic concepts of programming in embedded system using C.
- Illustrate the 8051 Microcontroller Family
- Develop the methods of Reading Switches
- Develop the structure using Object-oriented programming with C
- Identifythe Real-Time Constraints and case studies

UNIT-I: Programming Embedded Systems in C

Introduction, What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

Introducing the 8051 Microcontroller Family

Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements, Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption, Conclusions

UNIT-II: Reading Switches

Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), the need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT-III: Adding Structure to the Code

Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT-IV: Meeting Real-Time Constraints

Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT-V: Case Study-Intruder Alarm System

Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:

1. Embedded C - Michael J. Pont, 2nd Ed., Pearson Education, 2008.

REFERENCE BOOKS:

1. PIC MCU C-An introduction to programming, The Microchip PIC in CCS C – Nigel Gardner.

Elective-I DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

Course Outcome:

The student will be able to

- Apply the FFT algorithm for solving the DFT of a given signal.
- Describe the computational accuracy.
- Describe the features and Architectures for Programmable DSP Devices.

UNIT-I:Introduction to Digital Signal Processing: Introduction, a Digital signal processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT-II

Architectures for Programmable DSP Devices Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT-III

Programmable Digital Signal Processors Commercial Digital signal processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT-IV

Analog Devices Family of DSP Devices Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor.

Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT-V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.

2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009

3. Digital Signal Processors, Architecture, Programming and Applications- B. Venkataramani and M. Bhaskar, 2002, TMH

REFERENCE BOOKS:

1.Embedded Signal Processing with the Micro Signal Architecture: Woon-SengGan, Sen M. Kuo, Wiley-IEEE Press, 2007.

2. DSP Processor Fundamentals, Architectures & Features – Lapsleyetal. 2000, S. Chand & Co.

3. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI

4. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997

Elective-I SYSTEM ON CHIP

Course Outcome:

The student will be able to

- Describe SOC System Approach, design and its Architecture.
- Describe Memory Design for SOC
- Explain the concepts of bus models and Interconnect Architectures
- Describe Application Studies and Case Studies

UNIT-I:

Introduction to the System Approach System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT-II:

Processors Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT-III:

Memory Design for SOC Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT-IV:

Interconnect Customization and Configuration Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT-V:

Application Studies / Case Studies SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.Concepts of IP (Intellectual Property) cores and integration in SOC.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.

2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer

2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.

3. System on Chip Verification – Methodologies and Techniques – PrakashRashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

Elective-I SOFT COMPUTING TECHNIQUES

Course Outcome:

The student will be able to

- Describe Artificial Neural Networks, Fuzzy Logic System modeling and control
- Describe Genetic Algorithm
- Apply Neural Networks in different areas using MATLAB

UNIT –I: Introduction:

Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT –II: Artificial Neural Networks:

Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT –III: Fuzzy Logic System:

Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT –IV: Genetic Algorithm:

Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and anD-colony search techniques for solving optimization problems.

UNIT –V: Applications:

GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems.

TEXT BOOKS:

1. Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House, 1999.

2. Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994.

REFERENCE BOOKS:

1. Fuzzy Sets, Uncertainty and Information - Klir G.J. &Folger T.A., Prentice-Hall of India Pvt. Ltd., 1993.

2. Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994.

3. Introduction to Fuzzy Control - Driankov, Hellendroon, Narosa Publishers.

4. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.

5. Elements of Artificial Neural Networks - KishanMehrotra, Chelkuri K. Mohan, Sanjay Ranka, Penram International.

6. Artificial Neural Network –Simon Haykin, 2nd Ed., Pearson Education.

7. Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi.

ELECTIVE-II DIGITAL DESIGN USING HDL

Course Outcome:

The student will be able to

- Describe the basic concepts of Hardware Description Languages.
- Develop programs for Combinational and Sequential Logic Circuits HDL
- Construct the synthesis of Digital Logic Circuit Design
- Describe Testing of Digital Logic Circuits and CAD Tools

UNIT-I: Digital Logic Design using VHDL

Introduction, designing with VHDL, design entry methods, logic synthesis, entities, architecture, packages and configurations, types of models: dataflow, behavioral, structural, signals vs. variables, generics, data types, concurrent vs. sequential statements, loops and program controls. Digital Logic Design using Verilog HDL Introduction, Verilog Data types and Operators, Binary data manipulation, Combinational and Sequential logic design, Structural Models of Combinational Logic, Logic Simulation, Design Verification and Test Methodology, Propagation Delay, Truth Table models using Verilog.

UNIT-II: Combinational Logic Circuit Design using VHDL

Combinational circuits building blocks: Multiplexers, Decoders, Encoders, Code converters, Arithmetic comparison circuits, VHDL for combinational circuits, Adders-Half Adder, Full Adder, Ripple-Carry Adder, Carry Look-Ahead Adder, Subtraction, Multiplication. Sequential Logic Circuit Design using VHDL Flip-flops, registers & counters, synchronous sequential circuits: Basic design steps, Mealy State model, Design of FSM using CAD tools, Serial Adder Example, State Minimization, Design of Counter using sequential Circuit approach.

UNIT-III: Digital Logic Circuit DesignExamples using Verilog HDL

Behavioral modeling, Data types, Boolean-Equation-Based behavioral models of combinational logics, Propagation delay and continuous assignments, latches and level-sensitive circuits in Verilog, Cyclic behavioral models of flip-flops and latches and Edge detection, comparison of styles for behavioral model; Behavioral model, Multiplexers, Encoders and Decoders, Counters, Shift Registers, Register files, Dataflow models of a linear feedback shift register, Machines with multi cycle operations, ASM and ASMD charts for behavioral modeling, Design examples, Keypad scanner and encoder.

UNIT-IV: Synthesis of Digital Logic Circuit Design:

Introduction to Synthesis, Synthesis of combinational logic, Synthesis of sequential logic with latches and flip-flops, Synthesis of Explicit and Implicit State Machines, Registers and counters.

UNIT-V: Testing of Digital Logic Circuits and CAD Tools :

Testing of logic circuits, fault model, complexity of a test set, path-sensitization, circuits with tree structure, random tests, testing of sequential circuits, built in self test, printed circuit boards, computer aided design tools, synthesis, physical design.

TEXT BOOKS:

1. Stephen Brown &ZvonkoVranesic, “Fundamentals of Digital logic design with VHDL”, Tata McGraw Hill,2nd edition.

2. Michael D. Ciletti, “Advanced digital design with the Verilog HDL”, Eastern economy edition, PHI.

REFERENCE BOOKS:

1. Stephen Brown &ZvonkoVranesic, “Fundamentals of Digital logic with Verilog design”, Tata McGraw Hill,2nd edition.

2. Bhaskar, “VHDL Primer”,3rd Edition, PHI Publications.

3. Ian Grout, “Digital systems design with FPGAs and CPLDs”, Elsevier Publications.

ELECTIVE-2 CPLD AND FPGA ARCHITECURES AND APPLICATIONS

Course Outcome:

The student will be able to

- Describe the Programmable Logic Devices
- Distinguish the various types of Field Programmable Gate Arrays
- Apply the typical applications on FPGAs

UNIT-I: Introduction to Programmable Logic Devices

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices –Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II: Field Programmable Gate Arrays

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT –III: SRAM Programmable FPGAs:

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT –IV: Anti-Fuse Programmed FPGAs

Introduction, Programming Technology, Device Architecture, TheActel ACT1, ACT2 and ACT3 Architectures.

UNIT –V: Design Applications

General Design Issues, Counter Examples, A Fast Video Controller, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.

2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.

2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/ SamihaMourad, Pearson Low Price Edition.

3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.

4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

ELECTIVE-2 Algorithms for VLSI Design Automation

Course Outcome:

The student will be able to

- Describe Logic Synthesis
- Discuss VLSI Automation Algorithms
- Identify Placement, Floor Planning & Pin Assignment and Routing techniques

UNIT-I: Logic Synthesis & Verification:

Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

UNIT-II: VLSI Automation Algorithms:

Partitioning: Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

UNIT-III: Placement, Floor Planning & Pin Assignment:

Problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment

UNIT-IV: Global Routing:

Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches

UNIT-V: Detailed Routing:

problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms. Over The Cell Routing & Via Minimization: Two layers over the cell routers, constrained & unconstrained via minimization.

REFERENCE BOOKS:

1. NaveedShervani, “Algorithms for VLSI physical design Automation”, Kluwer Academic Publisher, Second edition.

2. ChristophnMeinel& Thorsten Theobold, “Algorithm and Data Structures for VLSI Design”, KAP, 2002.

3. Rolf Drechsheler : “Evolutionary Algorithm for VLSI”, Second edition

4. Trimburger, “Introduction to CAD for VLSI”, Kluwer Academic publisher, 2002 .

Elective –IIVLSI SIGNAL PROCESSING

Course Outcome:

The student will be able to

- Describe digital signal processing algorithms and processing.
- Distinguish folding and unfolding algorithms.
- Explain systolic architectures
- Explain various convolution algorithms.
- Describe applications of DSP processor in low power design.

UNIT-I:

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms.

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power.

Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques.

UNIT-II:

Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems

Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT-III:

Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT-IV:

Fast Convolution: Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT-V:

Low Power Design: Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA

VLSI LABORATORY

PART-A: VLSI Lab (Front-end Environment)

--The students are required to design the logic circuit to perform the followingexperiments using necessary simulator (Xilinx ISE Simulator/ Mentor GraphicsQuesta Simulator) to verify the logical /functional operation and to perform theanalysis with appropriate synthesizer (Xilinx ISE Synthesizer/Mentor GraphicsPrecision RTL) and then verify the implemented logic with different hardwaremodules/kits (CPLD/FPGA kits).

--The students are required to acquire the knowledge in both the Platforms (Xilinxand Mentor graphics) by perform at least Five experiments on each Platform.

List of Experiments:

1. Adder-Substractor.
2. Priority Encoder.
3. LFSR
4. Synchronous RAM.
5. ALU.
6. Up Counter/Down Counter.
7. Fire Detection and Control System using Combinational Logic circuits.
8. Traffic Light Controller using Sequential Logic circuits
9. Pattern Detection using Moore Machine.
10. Finite State Machine (FSM) based logic circuit.

PART-A: VLSI Lab (Back-end Environment)

--The students are required to design and implement the Layout of the following experiments of any Five using CMOS 130nm Technology with Mentor Graphics Tool.

List of Experiments:

1. Inverter Characteristics.
2. Full Adder.
3. RS-Latch, D-Latch and Clock Divider.
4. Synchronous Counter and Asynchronous Counter.
5. Static and Dynamic RAM.
6. ROM
7. Differential Amplifier.
8. Ring Oscillator
9. Digital-to-Analog-Converter.
10. Analog-to-Digital Converter.

Lab Requirements:

Software: Xilinx ISE Suite, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Mentor Graphics Back End/Tanner Software tool.

Hardware: Personal Computer with necessary peripherals, configuration and operating Systemand relevant VLSI (CPLD/FPGA) hardware Kits.

Semester -II

DESIGN FOR TESTABILITY

Course Outcome:

The students will be able to

- Interpret the concepts of modeling digital circuits and simulation.
- Describe modeling of faults and its testing for SSF.
- Explain various techniques of testing.

UNIT-I: Modeling:

Modeling digital circuits at logic level, register level and structural level. Levels of modeling.

Logic Simulation: Types of simulation, delay models, element evaluation, hazard detection, gate level event driven simulation.

UNIT-II: Fault Modeling:

Logic fault models, fault detection and redundancy, fault equivalence and fault location. Single stuck and multiple stuck – fault models. Fault simulation applications, general techniques for combinational circuits.

UNIT-III: Testing for Single Stuck Faults (SSF):

Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, functional testing with specific fault models. Vector simulation – ATPG vectors, formats, compaction and compression, selecting ATPG tool.

UNIT-IV: Design for Testability:

Testability trade-offs, techniques. Scan architectures and testing – controllability and observability, generic boundary scan, fully integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT-V: Built-in-Self-Test (BIST):

BIST concepts and test pattern generation, specific BIST architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level.

Reference Books

1. MironAbramovici, Melvin A.Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.

2. Michael L.Bushnell, VishwaniD.Agrawal, Essentials of Electronic Testing, Springer, 2000.
3. Michael D.Ciletti, Modeling, Synthesis, and Rapid Prototyping with the Verilog HDL., Prentice Hall, 1999.

CMOS DIGITAL IC DESIGN

Course Outcome:

The student will be able to

- Describe the concepts of MOS design.
- Demonstrate the combinational, sequential and dynamic CMOS logic circuits.
- Explain various semiconductor memories.

UNIT-I: MOS Design

NMOS & Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low Voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time; CMOS logic - Inverter, logic gates.

UNIT-II: Combinational MOS Logic Circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III: Sequential MOS Logic Circuits

Behaviour of bistable elements, Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-IV: Dynamic Logic Circuits

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits – Domino logic, NORA logic.

UNIT-V: Semiconductor Memories

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.

2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin,CRC Press, 2011

2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan,BorivojeNikolic, 2nd Ed., PHI.

EMBEDDED SYSTEM DESIGN - II

Course Outcome:

The student will be able to

- Describe the ARM architecture and its memory management.
- Apply instruction set for Arm programming.
- Develop basic ARM programs using C.
- Describe the concepts of memory management.

UNIT-I:

ARM Architecture ARM Design Philosophy, Registers, PSR, Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.Introduction to ARM Cortex.

UNIT-II:

ARM Programming Model-I Instruction Set: Data Processing Instructions, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT-III:

ARM Programming Model-II Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions.

UNIT-IV:

ARM Programming: Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT-V:

Memory Management Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Content Switch.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

2. ARM System-on-chip Architecture- Stephen Bo Furber - Addison-Wesley, 2000

REFERENCE BOOKS:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

EMBEDDED REAL TIME OPERATING SYSTEMS

Course Outcome:

The student will be able to

- Describe the concepts of real time operating system.
- Explain various RTOS and their programming concepts.
- Express program modeling for case studies.
- Construct an image for a target board.
- Describe RT Linux

UNIT-I: Introduction

OS Services, Process Management, Timer Functions, Event Functions, Memory Management, Device, File and IO Systems Management, Interrupt Routines in RTOS Environment and Handling of Interrupt Source Calls, Inter Process communication Functions, Real-Time Operating Systems, Basic Design Using an RTOS, RTOS Task Scheduling Models, Interrupt Latency and Response of the Tasks as Performance Metrics, OS Security Issues.

UNIT-II: RTOS Programming

Basic Functions and Types of RTOS for Embedded Systems, RTOS mCOS-II, RTOS Vx Works, Programming concepts of above RTOS with relevant Examples, Programming concepts of RTOS Windows CE, RTOS OSEK, RTOS Linux 2.6.x and RTOS RT Linux.

UNIT-III: Program Modeling – Case Studies

Case study of embedded system design and coding for an Automatic Chocolate Vending Machine (ACVM) Using Mucos RTOS, case study of digital camera hardware and software architecture, case study of coding for sending application layer byte streams on a TCP/IP Network Using RTOS Vx Works, Case Study of Embedded System for an Adaptive Cruise Control (ACC) System in Car, Case Study of Embedded System for a Smart Card, Case Study of Embedded System of Mobile Phone Software for Key Inputs.

UNIT-IV: Target Image Creation & Programming in Linux

Off-The-Shelf Operating Systems, Operating System Software, Target Image Creation for Window XP Embedded, Porting RTOS on a Micro Controller based Development Board. Overview and programming concepts of Unix/Linux Programming, Shell Programming, System Programming.

UNIT-V: Programming in RT Linux

Overview of RT Linux, Core RT Linux API, Program to display a message periodically, semaphore management, Mutex, Management, Case Study of Appliance Control by RT Linux System.

TEXT BOOKS:

1. Dr. K.V.K.K. Prasad: "Embedded/Real-Time Systems" Dream Tech Publications, Blackpad book.

2. Rajkamal: "Embedded Systems-Architecture, Programming and Design", Tata McGraw Hill Publications, Second Edition, 2008.

REFERENCES:

1. Labrosse, "Embedding system building blocks ", CMP publishers.

2. Rob Williams," Real time Systems Development", Butterworth Heinemann Publications.

ELECTIVE-III Low Power VLSI Design

Course Outcome:

The students will be able to

- Identify various sources of power consumption
- Estimate the power consumption sing simulation and probabilistic approaches.
- Discuss low power design at various levels of abstraction.
- Discuss clock distribution for low power dissipation.

UNIT-I: Introduction

Need for low power VLSI chips, Sources of power dissipation. Emerging Low power approaches. Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

UNIT-II: Power estimation Simulation Power analysis:

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation.

Probabilistic power analysis:

Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

UNIT-III: Low Power Design Circuit level:

Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

Logic level:

Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

UNIT-IV: Low power Architecture & Systems:

Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

UNIT-V: Low power Clock Distribution:

Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

Algorithm &architectural level methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

TEXTBOOKS:

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002

2. Rabaey, Pedram, “Low power design methodologies” Kluwer Academic, 1997

REFERENCES BOOKS:

1. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000

ELECTIVE-III CMOS MIXED SIGNAL CIRCUIT DESIGN

Course Outcome:

The students will be able to

- Design Mixed signal based circuits starting from basics constraints to advanced constraints.
- Analyze and design filter architectures using switched capacitor integrator circuits.
- Design circuits like PLL,A/D and D/A converters.
- Design over sampling circuits and higher order modulators.

UNIT-I: Switched Capacitor Circuits

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, bi quad filters.

UNIT-II: Phased Lock Loop (PLL)

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Dead zone, Jitter in PLLs; applications.

Unit III: Sampling Circuits

Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-and-Hold Architectures- Open-loop & closed-loop architectures, open-loop architecture with miller capacitance, multiplexed-input architectures, recycling architecture, switched capacitor architecture, current-mode architecture.

UNIT-IV: D/A Converters

Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT-V: A/D Converters

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2016

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Describeing Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

ELECTIVE-III

SYSTEMVERILOG

Course Outcome:

The students will be able to

- Describe data types, RTL models and rules in SystemVerilog.
- Demonstrate user defined, enumerated data types and structures in SystemVerilog.
- Explain the procedural blocks, FSM and interfaces in SystemVerilog.

UNIT-I: Introduction to SystemVerilog:

SystemVerilog Declaration Spaces: Packages, unit compilation-unit declarations, Declarations in unnamed statement blocks, Simulation time units and precision

SystemVerilog Literal Values and Built-in Data Types

Enhanced literal value assignments, ‘define enhancements, SystemVerilog variables, Using 2-state types in RTL models, Relaxation of type rules, Signed and unsigned modifiers, Static and automatic variables, Deterministic variable initialization, Type casting

UNIT-II: SystemVerilog User-Defined and Enumerated Types

User-defined types, Enumerated types

SystemVerilog Arrays, Structures and Unions Structures, Unions, Arrays, The for each array looping construct, Array querying system functions, The bits “size of” system function, Dynamic arrays, associative arrays, sparse arrays and strings

UNIT-III: SystemVerilog Procedural Blocks, Tasks and Functions

Verilog general purpose always procedural block, SystemVerilog specialized procedural blocks, Enhancements to tasks and functions

UNIT-IV: SystemVerilog Procedural Statements

New operators, Operand enhancements, Enhanced for loops, Bottom testing do...while loop, The for each array looping construct, Enhanced block names, Statement labels, Enhanced case statements, Enhanced if...else decisions

Modeling Finite State Machines with SystemVerilog

Modeling state machines with enumerated types, Using 2-state types in FSM models

UNIT-V: SystemVerilog Interfaces

Interface concepts, Interface declarations, Using interfaces as module ports, Instantiating and connecting interfaces, Referencing signals within an interface, Interface mod ports, Using tasks and functions in interfaces, Using procedural blocks in interfaces, Reconfigurable interfaces, Verification with interfaces

TEXTBOOKS:

1. Sutherland, " Systemverilog for Design", Springer publications

2. Christian B Spear, "SystemVerilog for Verification: A guide to learning the Testbench language features", Springer publications, 3 rd edition.

3. VijayaRaghavan, "SystemVerilog Assertions", Springer publications, 2005

ELECTIVE-III

SEMICONDUCTOR MEMORY DESIGN AND TESTING

Course Outcome:

The students will be able to

- Describe concepts of volatile and non volatile memory technologies.
- Discuss the fault modeling and testing memory devices.
- Explain the reliability and radiation effects of memory devices.
- Describe the advanced memory technologies.

UNIT-I: Random Access Memory Technologies

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT-II: Non-volatile Memories

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture.

UNIT-III: Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance

RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, nonvolatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory.

UNIT-IV: Semiconductor Memory Reliability and Radiation Effects

General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation. Dosimetry, Water Level Radiation Testing and Test structures.

UNIT-V: Advanced Memory Technologies and High-density Memory Packing Technologies

Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

TEXT BOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.

2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.

3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall.

ELECTIVE-IV

HARDWARE SOFTWARE CO-DESIGN

Course Outcome:

The students will be able to

- Describe co-design architectures, methods and algorithms.
- Describe prototyping emulation and target architecture using embedded systems.
- Explain the compilation techniques.
- Distinguish the various design specifications and verifications.
- Describe the system level specifications and design using languages.

UNIT-I: Co- Design Issues:

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT-II:

Prototyping and Emulation Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT-III:

Compilation Techniques and Tools for Embedded Processor Architectures Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT-IV:

Design Specification and Verification Design, co-design, the co-design computational model, concurrency coordinating con current computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT-V:

Languages for System-Level Specification and Design-I System-level specification, design representation for system level synthesis, system level specification languages.

Languages for System-Level Specification and Design-II

Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – JorgenStaunstrup, Wayne Wolf – 2009, Springer.

2. Hardware / Software Co- Design - Giovanni De Micheli, MariagiovannaSami, 2002, Kluwer Academic Publishers.

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R.Schaumont - 2010 – Springer Publications.

ELECTIVE-IV

EMBEDDED COMPUTING

Course Outcome:

The students will be able to

- Apply the concepts of Linux OS and programming
- Describe the different software development tools and interfacing modules
- Discuss the networking basics
- Describe the IA32 instruction set

UNIT – I:

Programming on Linux Platform:

System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box. **Operating System Overview**: Processes, Tasks, Threads, Multi-Threading, Semaphore, Message Queue.

UNIT – II:

Introduction to Software Development Tools:

GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools.

UNIT – III:

Interfacing Modules:

Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

UNIT – IV:

Networking Basics:

Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.

UNIT – V:

IA32 Instruction Set: application binary interface, exception and interrupt handling, interruptlatency, assemblers, assembler directives, macros, simulation and debugging tools.

TEXT BOOKS:

1. Peter Barry and Patrick Crowley, “Modern Embedded Computing”,1st Edition. Elsevier/Morgan Kaufmann, 2012.

2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.

3. Assembly Language for x86 Processors by Kip R. Irvine

4. Intel® 64 and IA-32 Architectures Software Developer Manuals

REFERENCE BOOKS

1. Abraham Silberschatz, Peter B. Galvin and Greg Gagne, “Operating System Concepts”, Wiley

2. Maurice J. Bach, “The Design of the UNIX Operating System”, Prentice-Hall

3. W. Richard Stevens, “UNIX Network Programming”, Pearson

ELECTIVE-IV

DESIGN FOR INTERNET OF THINGS

Course Outcome:

The student will be able to

- Describe M2M and IOT technologies
- Identify the layers and protocols in IOT
- Describe various communication technologies used in IOT
- Demonstrate various hardware components required for IOT applications

UNIT I – INTRODUCTION

Introduction from M2M to IoT, M2M and IoT Technology Fundamentals - Devices and gateways.IoT - An Architectural Overview – Building architecture, Main design principles and needed capabilities.

UNIT II – IOT PROTOCOLS

Functionality of Layers in IoT –Study of protocols - WirelessHART, Z-Wave, 6LoWPAN, RPL, CoAP, MQTT, oneM2M, ETSI M2M.

UNIT III COMMUNICATION TECHNOLOGIES IN IOT

IoT Connectivity – IEEE 802.15.4, WiFi, Bluetooth, Zigbee, Short Range Communications, LPWAN, Cellular Systems, Challenges and Solutions in 5G Era.

UNIT IV SYSTEM HARDWARE AND PROTOTYPING

Sensors, Actuators, Radio Frequency Identification, Wireless Sensor Networks and Participatory Sensing Technology, Prototyping the Embedded Devices for IoTs.

UNIT V – IOT APPLICATIONS

BUILDING IoT Application WITH RASPBERRY PI - Physical device – Raspberry Pi Interfaces – Programming – APIs / Packages – Web services, Real time applications of IoT-Connecting IoT to cloud – Cloud Storage for IoT.**Case Studies** - Smart and Connected Cities, Public Safety.

TEXTBOOKS:

1. Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stefan Avesand, StamatisKarnouskos, David Boyle, “From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence”, 1 st Edition, Academic Press, 2014.

2. IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry, Cisco Press 800 East 96th Street Indianapolis, Indiana 46240 USA

3. Daniel Minoli, “Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M2M Communications”, ISBN: 978-1-118- 47347-4, Willy Publications

4. IOT (Internet of Things) Programming: A Simple and Fast Way of Learning IOT by David Etter(Author)

5. Internet of Things - By Raj Kamal, McGraw-Hill Education. Copyright.

REFERENCE BOOKS:

1. From Internet of Things to Smart Cities: Enabling Technologies - edited by Hongjian Sun, Chao Wang, Bashar I. Ahmad, CRC Press -2018.

2. Peter Waher, “Learning Internet of Things”, PACKT publishing, BIRMINGHAM

3. Bernd Scholz-Reiter, Florian Michahelles, “Architecting the Internet of Things”, ISBN 978-3-642-19156-5 e-ISBN 978-3-642-19157-2, Springer

4. Vijay Madisetti and ArshdeepBahga, “Internet of Things (A Hands-on- Approach)”, 1 st Edition, VPT, 2014.

ELECTIVE IV

SOFTWARE FOR EMBEDDED SYSTEMS

Course outcomes:

The student will be able to

- Describe the fundamentals of embedded Programming.
- Describe the GNU C Programming Tool Chain in Linux.
- Explain time driven architecture, Serial Interface with a case study.
- Illustrate the concepts of embedded Java for Web Enabling of systems.

UNIT I EMBEDDED PROGRAMMING

C and Assembly - Programming Style - Declarations and Expressions - Arrays, Qualifiers and Reading Numbers - Decision and Control Statements - Programming Process - More Control Statements - Variable Scope and Functions - C Preprocessor - Advanced Types – Simple Pointers - Debugging and Optimization – In-line Assembly.

UNIT II C PROGRAMMING TOOLCHAIN IN LINUX

C preprocessor - Stages of Compilation - Introduction to GCC - Debugging with GDB – The Make utility - GNU Configure and Build System - GNU Binary utilities - Profiling - using *gprof*- Memory Leak Detection with *valgrind*- Introduction to GNU C Library

UNIT III EMBEDDED C AND EMBEDDED OS

Adding Structure to 'C' Code: Object oriented programming with C, Header files for Project and Port, Examples. Meeting Real-time constraints: Creating hardware delays - Need for timeout mechanism - Creating loop timeouts - Creating hardware timeouts. Creating embedded operating system: Basis of a simple embedded OS, Introduction to sEOS, Using Timer 0 and Timer 1, Portability issue, Alternative system architecture, Important design considerations when using sEOS.

UNIT IV TIME-DRIVEN MULTI-STATE ARCHITECTURE AND HARDWARE

Multi-State systems and function sequences: Implementing multi-state (Timed) system - Implementing a Multi-state (Input/Timed) system. Using the Serial Interface: RS232 - The Basic RS-232 Protocol - Asynchronous data transmission and baud rates - Flow control – Software architecture - Using on-chip UART for RS-232 communication - Memory requirements – The serial menu architecture - Examples. Case study: Intruder alarm system.

UNIT V EMBEDDED JAVA

Introduction to Embedded Java and J2ME – Smart Card basics – Java card technology overview – Java card objects – Java card applets – working with APDUs – Web Technology for Embedded Systems.

TEXTBOOKS:

1. Steve Oualline, ‘Practical C Programming 3rd Edition’, O’Reilly Media, Inc, 2006.

2. Stephen Kochan, “Programming in C”, 3rd Edition, Sams Publishing, 2009.

3. Michael J Pont, “Embedded C”, Pearson Education, 2007.

4. Zhiqun Chen, ‘Java Card Technology for Smart Cards: Architecture and Programmer’s Guide’, Addison-Wesley Professional, 2000.

EMBEDDED SYSTEM DESIGN LABORATORY

1. The Students are required to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926 developer kits and ARM-Cortex.
2. The following experiments are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification. The programs developed for the implementation should be at the level of an embedded system design.
3. The students are required to perform THREE experiments from Part-I and ALL experiments from Part-II and Part-III.

List of Experiments:

Part-I: Experiments using ARM-926 with PERFECT RTOS

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Reader's Writer's Problem for concurrent Tasks.

Part-II Experiments on ARM-CORTEX processor using any open source RTOS.

(Coo-Cox-Software-Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.
2. Interface ADC and DAC ports with the Input and Output sensitive devices.
3. Sensor interface with ARM-Cortex processor

Part-III Experiments on Raspberry PI (RPI) & ESP8266

1. RPI interfacing with sensor.
2. Sensor data upload to cloud using RPI.
3. ESP8266 interfacing with sensor.
4. Sensor data upload to cloud using ESP8266.

Lab Requirements:

Software:

1. Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO-COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.
2. LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

3. Arduino IDE

4. Python

Hardware:

1. The development kits of ARM-926 Developer Kits, ARM-Cortex Boards, Raspberry PI Board and ESP 8266 Board

2. Serial Cables, Network Cables and recommended power supply for the board.

3. Sensors for interfacing.